CLAIMS

What is claimed is:

1. An automatic-bias amplifier circuit comprising:

an amplifier comprising an input, an output, and a signal path between and including the input and output of the amplifier, wherein the amplifier is coupled to a fixed-level DC voltage source; and

a feedback loop coupled between the signal path and a bias input of the amplifier, wherein the feedback loop comprises a power detector and a bias circuit,

wherein the power detector comprises an input coupled to the signal path, and is operable for sampling a first signal on the signal path and for outputting to the feedback loop an analog voltage signal reflective of the power of the first signal, and

wherein the bias circuit is on the feedback loop between the power detector and the bias input of the amplifier, and causes the amplifier to draw a quiescent current, from the fixed-level DC voltage source, that varies proportionally with the analog voltage signal.

2. The automatic-bias amplifier circuit of claim 1, wherein the power detector is coupled to the signal path at an internal node of the amplifier, said internal node being between, but exclusive of, the input and the output of the amplifier.

3. The automatic-bias amplifier circuit of claim 1, wherein the power detector is coupled to the signal path for sampling at a plurality of nodes of the amplifier.

4. The automatic-bias amplifier circuit of claim 3, wherein at least one of the plurality of nodes of the signal path to which the power detector is coupled is an internal node of the amplifier, said internal node being between, but exclusive of, the input and output of the amplifier.

5. The automatic-bias amplifier circuit of claim 1, wherein the power detector is coupled to the output of the amplifier.

6. The automatic-bias amplifier circuit of claim 1, wherein the amplifier comprises a plurality of amplifier stages and the power detector is coupled for sampling between a pair of the amplifier stages.

7. The automatic-bias amplifier circuit of claim 1, further comprising a voltage divider in the feedback loop between the power detector and the bias circuit, wherein a voltage of the analog voltage signal is divided by the voltage divider.

8. The automatic-bias circuit of claim 7, wherein the amplifier, the bias circuit, and the power detector are together on a single integrated circuit, and at least part of the voltage divider is external to the single integrated circuit.

9. The automatic-bias amplifier circuit of claim 1, further comprising a means in the feedback loop between the power detector and the bias circuit for shifting the voltage of the analog voltage signal.

10. The automatic-bias circuit of claim 1, wherein the amplifier, the bias circuit, and the power detector are together on a single integrated circuit, and at least part of the means for shifting the voltage of the analog voltage signal is external to the single integrated circuit.

11. The automatic-bias circuit of claim 1, further comprising a linearizer circuit in the feedback loop between the power detector and the bias circuit, wherein the analog voltage signal is linearized by the linearizer circuit.

12. The automatic-bias circuit of claim 1, wherein the bias circuit comprises a current mirror.

13. The automatic-bias circuit of claim 1, wherein the bias input is within a current mirror.

14. The circuit of claim 1, wherein the quiescent current includes a fixed-level portion and a continuously-varying portion.

15. The circuit of claim 1, wherein a transistor of the bias circuit is in a current mirror with a transistor of the amplifier, the current mirror having a non-unity current mirror ratio.

16. An automatic-bias amplifier circuit comprising:

an amplifier comprising an input, an output, and a signal path between and including the input and output of the amplifier;

a power detector comprising an input coupled to the signal path, said power detector being operable for sampling a first signal on the signal path and for outputting an analog voltage signal reflective of the power of the first signal; and

a bias circuit coupled between the amplifier and the power detector, wherein the bias circuit generates an analog current that varies proportionally with analog voltage signal, and mirrors the analog current into the amplifier as at least part of a quiescent current of the amplifier.

17. The automatic-bias amplifier circuit of claim 16, further comprising a voltage divider coupled between the power detector and the bias circuit, wherein the amplifier, the bias circuit, and the power detector are together on a single integrated circuit, and at least part of the voltage divider is external to the single integrated circuit.

18. The automatic-bias amplifier circuit of claim 16, further comprising a linearizer circuit coupled between the power detector and the bias circuit, wherein the linearizer circuit linearizes the analog voltage signal.

19. The automatic-bias circuit of claim 16, wherein the bias circuit also mirrors a fixed-level current into the amplifier, whereby the quiescent current of the amplifier includes a first portion based on the analog current and a second portion based on the fixed-level current.

20. A wireless communication device comprising:

a baseband processor, an antenna, and a signal path between the baseband processor and the antenna;

an amplifier comprising an input on the signal path, and an output on the signal path coupled to the antenna;

a fixed-level DC voltage source coupled to the amplifier;

a power detector operable for sampling an RF signal on the signal path and for outputting an analog voltage signal reflective of the power of the RF signal; and

a bias circuit coupled between the power detector and a bias input of the amplifier, wherein the bias circuit causes the amplifier to draw a quiescent current, from the fixed-level DC voltage source, that varies proportionally with the analog voltage signal.

21. The wireless communication device of claim 20, wherein the power detector is coupled for sampling at an internal node of the amplifier, said internal node being on the signal path between, but exclusive of, the input and the output of the amplifier.

22. The wireless communication device of claim 21, wherein the amplifier comprises a plurality of amplifier stages, and the power detector is coupled for sampling between a pair of the amplifier stages.

23. The wireless communication device of claim 20, further comprising a preamplifier on the signal path between the baseband processor and the input of the amplifier, wherein the baseband processor provides a continuously varying voltage signal to the preamplifier to vary a gain of the preamplifier.

24. The wireless communications device of claim 23, wherein the baseband processor generates the continuously varying voltage signal provided to the preamplifier based on the analog voltage signal.

25. The wireless communication device of claim 21, wherein the bias circuit generates an analog current that varies proportionally to the analog voltage signal, and mirrors the analog current into the amplifier as at least part of the quiescent current.

26. The wireless communication device of claim 25, wherein the bias circuit also mirrors a fixed-level current into the amplifier, whereby the quiescent current of the amplifier includes a first portion derived from the analog current and a second portion derived from the fixed-level current.

27. A wireless communication device comprising:

a baseband processor, an antenna, and a signal path between the baseband processor and the antenna;

an amplifier comprising an input on the signal path, and an output on the signal path coupled to the antenna;

a power detector operable for sampling an RF signal on the signal path and for outputting an analog voltage signal reflective of the power of the RF signal; and

a bias circuit coupled between the power detector and a bias input of the amplifier, wherein the bias circuit controls a quiescent current of the amplifier based on the analog voltage signal.

28. A method comprising:

providing an amplifier on a signal path, said amplifier having an input on the signal path and an output on the signal path;

receiving a first signal on the signal path at the input of the amplifier, amplifying the first signal in the amplifier, and outputting the amplified first signal at the output of the amplifier;

detecting a power level of the first signal on the signal path at a sampling point of the amplifier selected from a group consisting of the output of the amplifier and an interior node of the amplifier, said interior node being between, but exclusive of, the input and the output of the amplifier;

generating an analog voltage signal reflective of the detected power level of the first signal; and

drawing a quiescent current in the amplifier from a fixed level DC power supply, said quiescent current varying proportionally with the analog voltage signal.

29. The method of claim 28, wherein the power level of the first signal is detected at least at one said interior node.

30. The method of claim 29, wherein the amplifier includes a plurality of amplifier stages on the signal path, and the power level of the first signal is detected at a said interior node between a pair of the amplifier stages.

31. The method of claim 28, wherein a preamplifier is on the signal path prior to the input of the amplifier, and further comprising:

determining a desired power level of the amplified first signal to be output by the amplifier;

adjusting a gain of the preamplifier so that the first signal received at the input of the amplifier will have a magnitude sufficient to be amplified by the amplifier to the desired power level.

32. The method of claim 31, wherein the gain of the preamplifier is adjusted based on the analog voltage signal.

33. The method of claim 28, wherein the method includes converting the analog voltage signal to an analog current that varies proportionally with the analog voltage signal, and mirroring the analog current into the amplifier as at least part of the quiescent current.

34. The method of claim 28, wherein the method includes drawing a fixed level current from the fixed-level DC power supply, and mirroring the fixed-level current into the amplifier, whereby the quiescent current of the amplifier includes a first portion based on the analog current and a second portion based on the fixed-level current.

35. The method of claim 28, wherein the first signal is an RF signal, and detecting the power level of the first signal comprises measuring an RF voltage.

36. The method of claim 28, wherein the first signal is an RF signal, and detecting the power level of the first signal comprises measuring an RF current.